What is Claimed:

1. A process for manufacturing an integrated circuit package comprising:

(a) providing a substrate having a first dielectric layer, a conductive layer above the first dielectric layer, and a second dielectric layer above the conductive layer, the second dielectric layer having a cavity exposing a portion of the conductive layer; and

(b) interconnecting an integrated circuit directly to the exposed portion of the conductive layer in the cavity.

2. The method of claim 1 wherein step (b) comprises:

coupling a conductor to a bond pad formed on the integrated circuit; and

connecting the conductor directly to the conductive layer.

3. The method of claim 1 further comprising providing one of a ground plane and a power plane in the exposed portion of the conductive layer.

4. The method of claim 3 further comprising providing at least one connection for a signal line in the exposed portion of the conductive layer.

5. The method of claim 1 further comprising providing at least one connection for a signal line in the exposed portion of the conductive layer.

6. The method of claim 1 further comprising forming multiple interconnections between the integrated circuit chip and the conductive layer.

7. A method of manufacturing a substrate adapted to receive an integrated circuit chip comprising:

(a) providing a first dielectric layer;

(b) providing a conductive layer above the first dielectric layer;

(c) providing a second dielectric layer above the conductive layer; and

(d) forming a cavity in the second dielectric layer to expose a portion of the conductive layer.

8. The method of claim 7 wherein steps (a), (b), and (c) occur prior to step (d).

9. The method of claim 7 further comprising:

providing a contact area to a ground plane by exposing the portion of the conductive layer.

10. The method of claim 7 further comprising:

(e) forming plated through holes in the substrate.

11. The method of claim 10 wherein step (e) is performed prior to step (d).

12. A method of manufacturing an integrated circuit package comprising:

providing the substrate of claim 7; and

coupling the integrated circuit chip to the substrate.

13. A method of manufacturing a substrate adapted to receive an integrated circuit chip comprising:

(a) providing a first dielectric layer;

(b) providing a first conductive layer above the dielectric layer;

(c) providing a second dielectric layer above the first conductive layer;

(d) providing a second conductive layer above the second dielectric layer;

(e) forming a cavity in a first region of the second dielectric layer to expose a portion of the first conductive layer.

14. The process of claim 13 wherein step (d) further comprises providing the second conductive layer on regions other than the first region.

15. The process of claim 13 wherein step (d) further comprises removing a portion of the conductive layer formed above the first region.

16. A method of manufacturing an integrated circuit package comprising:

providing the substrate of claim 13; and

coupling the integrated circuit chip to the substrate.

17. A process for manufacturing an integrated circuit package comprising:

(a) receiving a substrate having a first dielectric layer, a conductive layer above the first dielectric layer, and a second dielectric layer above the conductive layer, the second dielectric layer having a cavity exposing a portion of the conductive layer; and

(b) interconnecting an integrated circuit directly to the exposed portion of the conductive layer in the cavity.